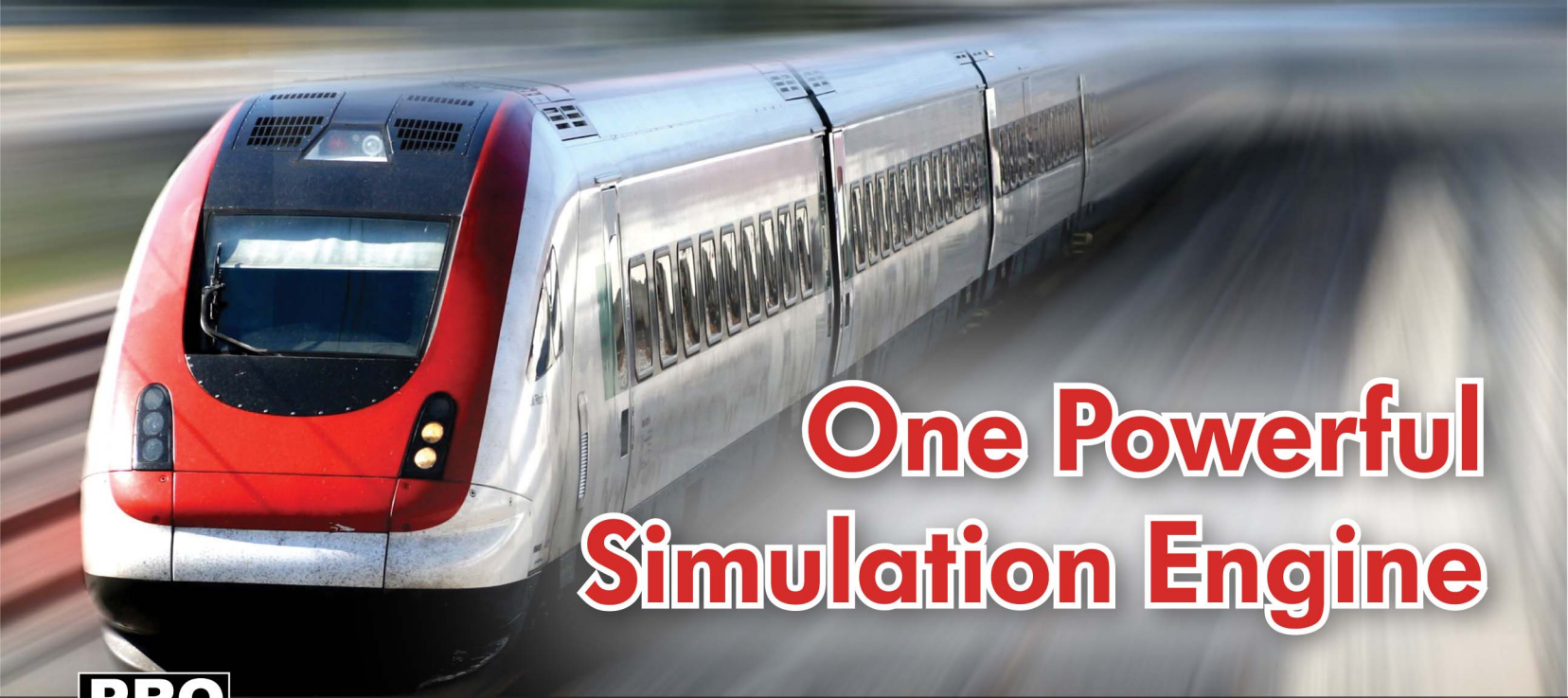

One Powerful Simulation Engine

Riviera-PRO

Riviera-PRO™ is a high-performance, mixed-language simulation engine with advanced debugging tools for ASIC and FPGA design teams. Riviera-PRO supports VHDL, Verilog® SystemVerilog, SystemC, C/C++, PSL and OVA assertions from one common design environment. Riviera-PRO enables mixed RTL debugging, long regression testing, timing simulation and electronic system level (ESL) verification.

Top Features

- Common-kernel mixed language simulator
- IEEE Standards Support (VHDL, Verilog®, SystemVerilog, SystemC)
- Universal HDL/SystemC code level debugging
- Assertion and coverage based verification
- DSP/HDL algorithm co-simulation
- Script compatible with other HDL simulators
- Multi-Platform (32/64bit Linux®, Solaris®, Windows®)

Advanced Verification Methodologies

Riviera-PRO supports powerful verification techniques like assertion based verification, transaction level modeling and constrained random test generation using SystemC, SystemVerilog and PSL. A powerful code coverage analyzer helps achieve 100% test coverage of all RTL statements, lines, signals and logical expressions in the design. An optional embedded lint tool checks for reliable, portable HDL code.

World Class Debugging Tools

Riviera-PRO provides highly intuitive, graphical debugging tools including a high performance waveform viewer and graphical dataflow for quickly tracing signal drivers/readers across multiple levels of design hierarchy and unknown values to their origin. Debug C/C++/SystemC with VHDL/SystemVerilog from either domain, set breakpoints and single-step through C code with full visibility into signals, call stack, register and memory contents at any level of hierarchy.

Compatible with Existing Verification Environment

Leverage your existing investment in tools and infrastructure by using a native Tcl command interface and aliasing at the command and switch levels. Riviera-PRO is virtually "drop-in" compatible with existing scripted verification environments. Additionally, Riviera-PRO is tightly integrated with dozens of popular EDA tools including, Denali®, Novas®, MATLAB®, Simulink® and Zuken® PCB tools.

STANDARDS

SystemVerilog

SYSTEMC™

accellera

SILICON

Actel®

ALTERA®

CHIP-X

Lattice Semiconductor Corporation

QuickLogic®

XILINX®

INTERFACES

ARM

cadence™

The MathWorks

Mentor Graphics®

NOVAS

Synplicity®

SYNOPSYS®

ZUKEN

FEATURES	PRODUCT CONFIGURATIONS		
Supported Languages	**LV**	**LVT**	**LVT-SV**
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	•	•	•
SystemVerilog IEEE 1800 (Design)	•	•	•
EDIF 2.0.0	•	•	•
SystemC™ 2.2 IEEE 1666/OSCI 2.2		•	•
PSL IEEE 1850		•	•
SystemVerilog IEEE 1800 (Assertions)		•	•
SystemVerilog IEEE 1800 (Verification)			•
Verification			
PSL Assertions and Coverage		•	•
OpenVera Assertions and Coverage		•	•
SystemVerilog Assertions and Coverage		•	•
Simulation			
Single or Mixed Language	•	•	•
External Programming Interfaces (PLI/VPI/VHPI)	•	•	•
Platform Independent Libraries	•	•	•
Simulation Model Protection/Library Encryption	•	•	•
Open IP Encryption; Verilog 1364-2005; VHDL 1076-2008	•	•	•
Verilog-RTL, Gate and Timing Optimization		•	•
VHDL RTL and Vital Optimization		•	•
Support for 64-bit Simulation Engine		•	•
Debug and Analysis			
Interactive Code Execution Tracing	•	•	•
Advanced Breakpoint Management	•	•	•
Accelerated Waveform and List Viewer (ASDB)	•	•	•
Waveform Compare and Memory Viewer	•	•	•
XTrace, Profiler and Signal Agent		•	•
Integrated Source Level C/SystemC Debugger		•	•
Advanced Dataflow		•	•
Synopsys® SmartModels®, SWIFT™ and LMTV		•	•
Novas® Debussy®		•	•
MATLAB® and Simulink® Co-simulation		•	•
Assertions Waveform Viewer		•	•
ALINT™ Design Rule Checker		Option	•
Coverage Tools			
Statement, Branch and Expression Coverage		•	•
Toggle Coverage		•	•
Design Entry and Design Management			
HDL and Text Editor	•	•	•
Language Assistant with Templates and Auto-complete	•	•	•
Design Manager	•	•	•
Tcl Scripting and Macro Language	•	•	•
Computer Platforms			
Supported Operating Systems: Linux® 32/64, Solaris®, Unix®, Microsoft® Windows® 2000/2003/XP/Vista			

Technology Patent no. 5,051,938; Simulation of selected logic circuit designs

HDL PRO ALINT HES

ALDEC
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