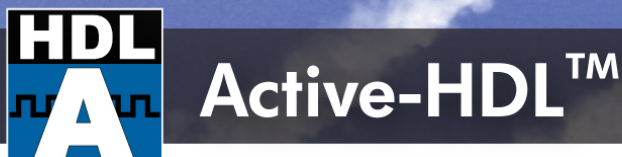


Integrated FPGA Design and Simulation

- Graphical Design Tools
- Mixed-Language Simulator
- Easy to Use



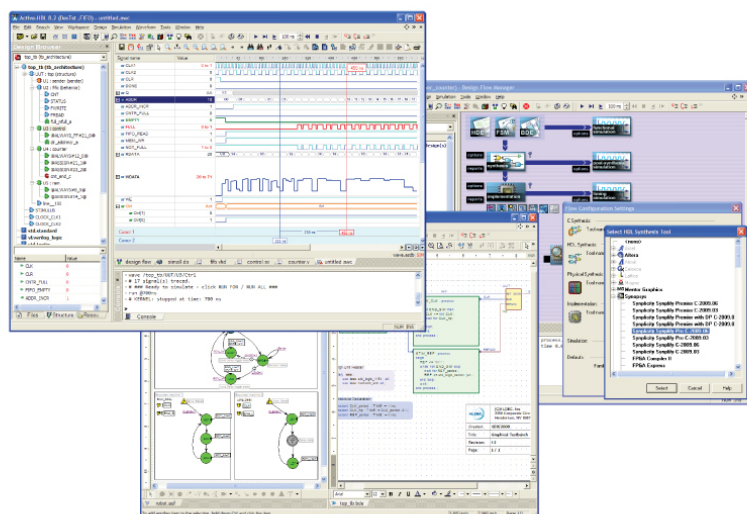
Active-HDL is an integrated FPGA Design and Simulation solution, providing a design entry, a high-performance mixed language simulator and a easy-to-use, multi-vendor FPGA flow manager that controls Simulation, Synthesis and Implementation for industry leading FPGA devices, such as Actel™, Altera®, Lattice®, Quicklogic®, Xilinx® and over 87 brand-leading EDA tools, all from one common environment.

Top Features

- Graphical Design Entry
- High Performance Mixed-Language HDL Simulator
- IEEE VHDL, Verilog, SystemVerilog (Design), SystemC
- Advanced Debugging & Code Coverage
- IP Encryption based on IEEE Standards
- ABV, Assertion-Based Verification
- DSP Co-simulation with MATLAB®/Simulink®
- PCB Design Interface
- HTML and PDF Design Documentation
- Windows® 2000/2003/XP/Vista

Graphical Design Entry

Draw powerful finite state machine diagrams and let the tool generate your synthesizable RTL code. Quickly connect all design modules at the top-level and output structural HDL using the built-in block diagram editor. Convert HDL to Graphics easily, with Code2Graphics™. Let Active-HDL import, re-target, enhance, simulate and debug Legacy Designs.



High Performance, Mixed Language Simulation

Active-HDL includes a high performance, common-kernel, mixed language simulator supporting batch mode simulation, VCD, performance profiler, memory viewer, encrypted IP and FPGA vendor libraries. Drive your system-level simulation model using complex testbenches or create quick and flexible stimulators to rapidly test design modules.

Debugging & Code Coverage

Active-HDL includes state-of-the-art debugging with an Accelerated Waveform, with cross-probing to HDL source code, breakpoint(s) management, testbench and stimulus generation. A powerful HDL code coverage analyzer provides 100% test coverage of all RTL statements, lines, signals, toggle, branch and logical expressions in the design.



STANDARDS



SILICON



INTERFACES



FEATURES

PRODUCT CONFIGURATIONS

Design Entry	DM	Designer Edition	PE	EE
HDL, Text, Block Diagram and State Machine Editor	•	•	•	•
Language Assistant with Templates and Auto-Complete	•	•	•	•
Macro, Tcl/Tk, Perl script Support	•	•	•	•
Pre-compiled FPGA Vendor Libraries	•	•	•	•
Code2Graphics™ Converter	•	•	•	•
Legacy Schematic Design Import and Symbol Import/Export	•	•	•	•
Supported Languages				
Single or Mixed Language Design Support	Mixed Only	Mixed Only	•	•
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•	•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	•	•	•	•
SystemVerilog IEEE 1800 (Design)	•	•	•	•
SystemC™ 2.2 IEEE 1666/OSCI 2.2/TLM 2.0			Option	•
Code Generation Tools				
Testbench Generation from Waveforms			•	•
Testbench Generation from State Diagram			•	•
Project Management				
Design Flow Manager for All FPGA Vendors	•	•	•	•
Revision Control Interface	•	•	•	•
Simulation/Verification				
Simulation Performance (Baseline 2X Faster than FPGA Vendor Supplied Simulator)		Baseline	3X Baseline	Up To 6X Baseline
Simulation Model Protection/Library Encryption		•	•	•
VHDL/Verilog IEEE compatible Encryption		•	•	•
Value Change Dump (VCD and Extended VCD) Support		•	•	•
Batch Mode Simulation/Regression (VSimSA)			•	•
Profiler (Performance Metrics)			Option	•
Verilog HDL Simulation Optimization				•
VHDL Simulation Optimization				•
HDL Debug and Analysis				
Interactive Code Execution Tracing		•	•	•
Advanced Breakpoint Management		•	•	•
Memory Viewer		•	•	•
Waveform Viewer (AWF and ASDB) + Editor		Viewer Only	•	•
Waveform Stimulator		•	•	•
Waveform Compare			•	•
Post Simulation Debug			•	•
C++ Debugger			•	•
Signal Agent (VHDL and Mixed Only)			•	•
X-Trace			Option	•
Advanced Dataflow			Option	•
Coverage Tools Bundle				
Statement, Code and Branch Coverage			Option	•
Toggle Coverage			Option	•
Expression and Condition Coverage			Option	•
Lint - Design Rule Checking				
Basic Lint (VHDL and Verilog)			Option	•
External Simulation Interface				
Synopsys SmartModels®, SWIFT™ Interface and LMTV			Option	•
SpringSoft® Verdi™ PSD mode Interface			Option	•
Co-Simulation				
Simulink® Co-Simulation			•	•
MATLAB® Co-Simulation			Option	•
Assertions				
PSL IEEE 1850 Assertions and Coverage				Option
SystemVerilog IEEE 1800 Assertions and Coverage				Option
OpenVera Assertions and Coverage				Option
Documentation				
Export to PDF/HTML/Bitmap Graphics	•		•	•
Advanced Export to PDF (Vector Graphics)	Option		•	•
Specialty Solutions				
PCB Interface			•	•
MiniSFM (Server Farm)			Option	Option
Supported Platforms				
Supported Operating Systems: Microsoft® Windows® 2000/2003/XP/Vista	•	•	•	•

Technology Patent no. 5,051,938; Simulation of selected logic circuit designs

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