

# Advanced Linting for Clean RTL Code



## HDL Linting Engine

**ALINT™** is a highly optimized HDL design rule checker. It includes a complete set of STARC Design Style Guide rules to use for next ASIC design. STARC is a consortium of 11 Japanese ASIC foundries that has established a set of design rule guidelines for corporations to follow based on a set of best-design practices.

Seasoned designers know that compiling, simulating and even synthesizing source code is not always the most challenging part of the design. To make the design work exactly as expected with reasonable cost, time and quality is what makes the difference between project success and failure.

### Top Features

- Source Code checks, design elaboration and synthesis emulation
- Clock Domain Crossing (CDC)
- User Modified Design Rules
- Fast analysis of complex ASIC/FPGA-SOC designs
- Cross-probing of error messages to source code
- Configuration Manager
- Supports STARC Design Rules

### Static and Dynamic Checking

ALINT enables both static and dynamic source code checking. The tool elaborates the entire design and emulates synthesis to help detect a larger number of potential design issues. Checks performed by ALINT are not theoretical—they are based on years of practical experience accumulated by leading Japanese silicon manufacturers working within the STARC consortium.

### STARC Rule Support

ALINT supports STARC Design Style Guide rules and allows for individual rule configuration, grouping rules in rule sets/policies and selecting active policies. The Application Programming Interface (API) allows creation of completely new rules and their easy incorporation into existing sets. The extensive set of predefined rules and flexible user defined configurability can help in all areas of design management: design for reuse, design for testability and optimization for synthesis and clock domain crossing (CDC) analysis.



## STANDARDS



## PARTNERS



## Design Preparation

Open ALINT configurator and select the set of rules most suitable for your design. If necessary, adjust parameters of individual rules to fine-tune design checking to meet requirements. Adjust options to execute only code checks for quick evaluation of your design or enable design elaboration for thorough evaluation.

## Analyze Design

Review messages created by ALINT. The error messages will provide you with a good understanding of what is taking place within your design. Utilize built-in cross probing and error detection to take you directly to the source code in which the error was detected.

## Analyze Results

## Configure the Design

The screenshot displays the ALINT tool interface. On the left, a 'Violation Report' table shows the following data:

Violations	Total	Error	Warning	Info
Files	4	0	28	0
Modules	4	0	4	0
Rulesets	0	0	1	0
Rules	28	0	28	0

The main window shows a code editor with a violation highlighted in red. The violation message at the bottom reads: 'ALINT: Warning: src/stage3\_elab\_analysis/cnv.v : (93, 1): instance 'top\_CONVERTER'. #STARC 2.8.1.6# BIT WIDTH '9' OF THE 'case' selection expression does not match the bit width '8' of all 'case' item(s). Match bit widths exactly to avoid simulation and synthesis difficulties. Level: Recommendation 2.'

## Run Linting

## Cross-Probing and Error Detection

ALINT includes a clear and informative set of messages that are generated during checking and a direct cross-link with the source code to ensure high efficiency of work and significantly shorten design schedule.

## Violation Viewer

Advance Violation Database, (AVDB) stores violation reports which can be filtered using combinations of criteria such as rule, severity, instance, source file and more. AVDB manages different project revisions and enables easy change tracking.

