H.264 BP VIDEO DECODER CORE

OVERVIEW

The AL-H264D-CTRL core is a feature rich RTL implementation of H.264/AVC Baseline Profile Decoder algorithm for high quality multimedia services on limited bandwidth network. The core processes video bitstream from external memory such as SRAM or DDR1/2 and writes decoded frames back to external memory. It supports video resolutions from SQCIF to HD.

Designed for easy reuse in ASIC and FPGA implementations, the design is strictly synchronous with positive-edge clocking. The implementation is completely programmable SoC solution. It is operable both in micro-code free hardwire mode or in SW assist mode in ARM embedded processor system.

The core decodes CIF @ 30fps with a single 12 MHz clock source. The design is a multi clock domain design with clock gating enabled to switch off and on certain modules and conserve power. The core is also designed for very low latency processing yet optimal gate count.

A single core can be employed to process multiple channels utilizing a simple software scheduler.

The core is tested with JM version 15.1 reference decoder. The core is proven on FPGA platform in ARM system. The design comes with verification suite, bit-accurate C model and user documentation.

APPLICATIONS

- Mobile phone, Handheld video
- Camera, Security systems
- Video game consoles, Mobile TV
- Blu-ray DVD players
- Satellite TV/IPTV/Cable Set-top-box
- Video conferencing
- HD enabled MID, netbook

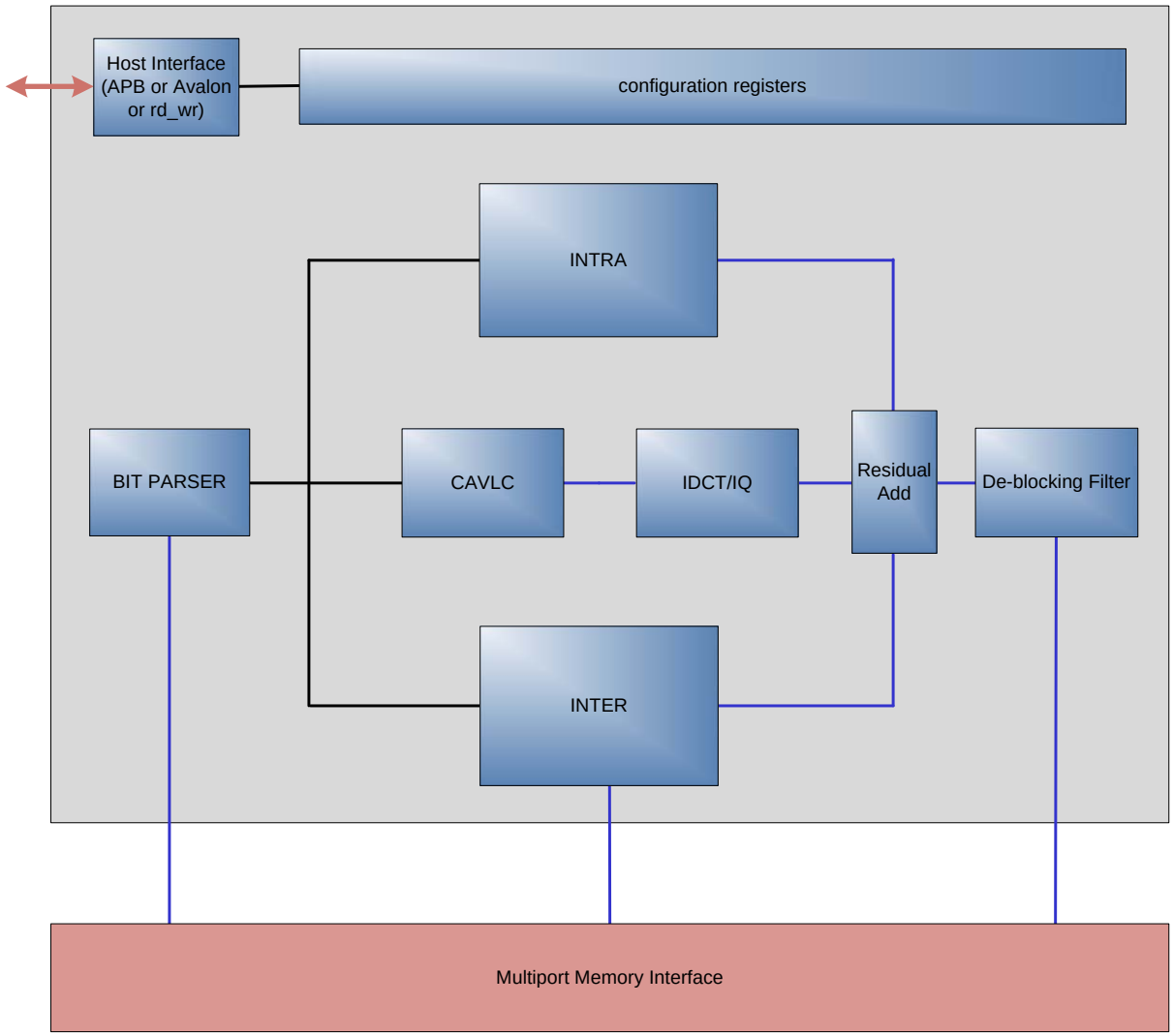
Features

- ✓ Compliant with ITU-T Recommendation H.264 ISO/IEC 14496-10 Advanced Video Coding Standard at Baseline profile up to Level 3.1.
- ✓ Support frame sizes from SQCIF (128x96 up to SVGA (800x600) on FPGA; and up to HD1080p on ASIC.
- ✓ The design can be configured and controlled through a set of registers visible through AMBA/AVALON bus architecture.
- ✓ Capable of decoding multiple streams simultaneously.
- ✓ Supports both Arbitrary Slice Ordering (ASO) and Flexible Macroblock Ordering (FMO) for error resilience and security.
- ✓ Supports skipped macroblock.
- ✓ Half-pel and quarter-pel motion compensation.
- ✓ Supports Motion vector range of -2048 to +2047.75 horizontal and -512.00 to +511.75 vertical.
- ✓ Supports up to 16 motion vectors (all permitted block sizes) per macroblock and over frame boundaries motion vectors for all resolutions.
- ✓ Supports all 4x4, all 16x16 luma and all chroma modes of intra prediction.
- ✓ In-loop de-blocking filter for better images.

SOFTWARE

Control plane software is available for the IP core when run in HW-SW mode. It is optimized for ARM Thumb instruction set. It can be easily ported to any other embedded CPU. Also, the entire H.264 SW decoder is available as a separate product.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The decoder consumes H.264 encoded NAL byte streams and outputs YUV 4:2:0 data. The NAL byte stream is fed to the decoder from DDR or SRAM memory. The bitstream parser block decodes NAL byte stream into control data and sends rest to residual decoding block. The

CAVLC and IDCT/IQ block takes in the remaining data from the NAL byte stream and produces residual data to be used with the predicted pixels from Intra/Inter prediction blocks. The intra or inter block uses control data from the bitstream parser and predicts pixel data. The intra block uses on-chip memory to use neighboring pixels for prediction while the inter block uses reference picture pixels that are fetched from the DDR memory to do the prediction. The predicted pixels and the residual pixels are then added and sent to the in-loop deblocking module. The deblocking filter then stores this data in DDR memory in raster scan which is display ready.

The SW can replace any HW module that is described above with a SW function. SW can also be used to orchestrate multi stream decoding and configuring the HW on the fly.

IMPLEMENTATION

The IP core is implemented in Altera Cyclone-III FPGA. Device utilization details are:

DEVICE	AREA	RAM	PERFORMANCE
Altera Cyclone III	50K LC	40 Kbits	Fmax = 120 MHz

DELIVERABLES

- HDL RTL source code or EDIF netlist for FPGA
- Self-checking Testbench in Verilog.
- Simulation scripts, vectors, expected results, and comparison utility
- Synthesis and STA scripts.
- Comprehensive user documentation, including detailed specifications and a system integration guide

ORDERING INFORMATION

Please contact the following office for evaluation and licensing questions.

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